19-1925; Rev 1; 6/01

Nonvolatile, Quad, 8-Bit DACs

General Description

The MAX5105/MAX5106 nonvolatile, quad, 8-bit digital-to-analog converters (DACs) operate from a single +2.7V to +5.5V supply. An internal EEPROM stores the DAC states even after power is removed. Data from these nonvolatile registers automatically initialize the DAC outputs and operating states during power-up. Precision internal buffers swing Rail-to-Rail®, and the reference input range includes both ground and the positive rail.

The MAX5105/MAX5106 feature a software-controlled 10µA shutdown mode and a mute state that drives the DAC outputs to their respective REFL_ voltages. The MAX5105 includes an asynchronous MUTE input, as well as a RDY/$\overline{BSY}$ output that indicates the status of the nonvolatile memory.

The MAX5105 is available in a 20-pin QSOP and 20-pin wide SO packages, and the MAX5106 is available in a 16-pin QSOP package.

Applications

Digital Gain and Offset Adjustments

Programmable Attenuators

Portable Instruments

Power-Amp Bias Control

Functional Diagram appears at end of data sheet.

Rail-to-Rail is a trademark of Nippon Motorola, Ltd.

SPI/QSPI are trademarks of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.

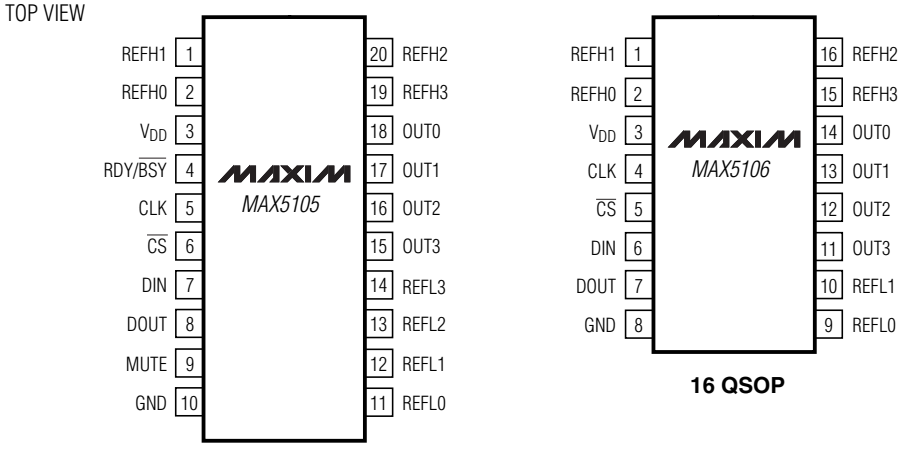
Features

- **On-Chip EEPROM Stores DAC States**
- **Power-On Reset Initialization of All Registers to Prestored States**
- **+2.7V to +5.5V Single-Supply Operation**
- **Four 8-Bit DACs with Independent High and Low Reference Inputs (MAX5105)**
- **Ground to V_{DD} Reference Input Range**
- **Rail-to-Rail Output Buffers**
- **Low 1mA Supply Current**
- **Low Power 10µA (max) Shutdown Mode**
- **Small 20- or 16-Pin QSOP Package**
- **SPI™/QSPI™/MICROWIRE™-Compatible Serial Interface**
- **Asynchronous MUTE Input (MAX5105)**
- **RDY/$\overline{BSY}$ Pin to Indicate Memory Status (MAX5105)**
- **Wide Operating Temperature Range (-40°C to +85°C)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5105EEP	-40°C to +85°C	20 QSOP
MAX5105EWP	-40°C to +85°C	20 SO
MAX5106EEE	-40°C to +85°C	16 QSOP

Pin Configurations



ABSOLUTE MAXIMUM RATINGS

V_{DD}, DIN, $\overline{CS}$, CLK, MUTE to GND .....-0.3V, +6V
DOUT, REFH_, REFL_, RDY/$\overline{BSY}$,
OUT_ to GND .....-0.3V to (V_{DD} + 0.3V)
Maximum Current into Any Pin .....±50mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C).....666.7mW
20-Pin QSOP (derate 9.1mW/°C above +70°C).....727.3mW
20-Pin SO (derate 10mW/°C above +70°C).....800mW
Operating Temperature Range
MAX510_ .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = $V_{REFH\_}$ = +2.7V to +5.5V, GND = $V_{REFL\_}$ = 0, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution			8			Bits
Integral Nonlinearity	INL	Code range 10hex to F0hex, I_{LOAD} = 50µA			±1	LSB
		Full code range, I_{LOAD} = 50µA			±2	
Differential Nonlinearity (Note 1)	DNL	Code range 10hex to F0hex, I_{LOAD} = 50µA			±0.5	LSB
		Full code range, I_{LOAD} = 50µA			±1	
Zero-Code Error	ZCE	Code = 0Ahex			±20	mV
Zero-Code Temperature Coefficient		Code = 0Ahex		±20		µV/°C
Gain Error (Note 2)		Code = F0hex			±1	LSB
Gain-Error Temperature Coefficient		Code = F0hex		±0.002		LSB/°C
Power-Supply Rejection Ratio	PSRR	Code = 0Ahex and FFhex, V_{DD} = 2.7V to 5.5V, $V_{REFH\_}$ = 2.5V, $V_{REFL\_}$ = 0, I_{LOAD} = 50µA			±1	LSB/V
REFERENCE INPUT						
Reference Input Voltage Range	$V_{REFH\_}$, $V_{REFL\_}$		0		V_{DD}	V
Input Resistance			92	256	413	kΩ
Input Resistance Matching				±0.2	±1	%
Input Capacitance				10		pF
DAC OUTPUTS						
Output Voltage Range		N = input code, I_{LOAD} = 0	$V_{REFL\_}$	(V_{REFH} - V_{REFL}) x (N/256) + $V_{REFL\_}$		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = $V_{REFH\_}$ = +2.7V to +5.5V, GND = $V_{REFL\_}$ = 0, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Current (Note 3)		$\Delta V_{OUT\_}$< 1LSB			±1.0		mA
Amplifier Output Resistance (Note 3)					3		Ω
DIGITAL INPUTS							
Input High Voltage	V_{IH}			0.7 x V_{DD}			V
Input Low Voltage	V_{IL}					0.8	V
Input Current	I_{IN}	V_{IN} = 0 or V_{DD}				±10	µA
Input Capacitance	C_{IN}				10		pF
DIGITAL OUTPUTS							
Output High Voltage	V_{OH}	I_{SOURCE} = 0.4mA		V_{DD} - 0.3			V
Output Low Voltage	V_{OL}	I_{SINK} = 1mA				0.4	V
Three-State Leakage Current	I_{LEAK}					±10	µA
Three-State Output Capacitance	C_{OUT}				15		pF
DYNAMIC PERFORMANCE							
CLK to OUT_ Settling Time (Note 4)	t_{COS}				6		µs
Channel-to-Channel Crosstalk (Note 5)		V_{DD} = +5V, code = Ffhex, $V_{REFH\_}$ = 2.5Vp-p at 10kHz			85		dB
Signal to Noise Plus Distortion	SINAD	V_{DD} = +5V, code = FFhex	$V_{REFH\_}$ = 2.5Vp-p at 1kHz		58		dB
			$V_{REFH\_}$ = 2.5Vp-p at 10kHz		56		
Multiplying Bandwidth		$V_{REFH\_}$ = 0.5Vp-p, 3dB bandwidth			250		kHz
Reference Feedthrough		V_{DD} = +5V, code = 00hex, $V_{REFH\_}$ = 2.5Vp-p at 1kHz			86		dB
Clock Feedthrough					4		nV - s
DAC Output White Noise					75		nV/√Hz
Shutdown Recovery Time	t_{SDR}				7		µs
Time to Shutdown	t_{SHDN}				2		µs
POWER SUPPLIES							
Supply Voltage	V_{DD}			2.7		5.5	V
Supply Current	I_{DD}	I_{LOAD} = 0, digital inputs at GND or V_{DD}			0.8	1.0	mA
		During nonvolatile write operation			20		
Shutdown Current					0.5	10	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = $V_{REFH\_}$ = +2.7V to +5.5V, GND = $V_{REFL\_}$ = 0, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL TIMING						
CLK Period	t_{CP}		1			µs
CLK High Time	t_{CH}		300			ns
CLK Low Time	t_{CL}		300			ns
$\overline{CS}$ High Time	t_{CSHT}		150			ns
$\overline{CS}$ Setup Time	t_{CSS}		100			ns
$\overline{CS}$ Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		100			ns
DIN Hold Time	t_{DH}		0			ns
CLK to DOUT Valid Time	t_{CDV}	C_{LOAD} = 100pF			1	µs
CLK to DOUT Propagation Delay	t_{CD}	C_{LOAD} = 100pF			1	µs
DOUT Disable Time	t_{CSD}	C_{LOAD} = 100pF			250	ns
Nonvolatile Store Time	t_{BUSY}				13	ms
NONVOLATILE MEMORY RELIABILITY						
Data Retention		MIL STD-883 Test Method 1008		100		Years
Endurance		MIL STD-883 Test Method 1033		100,000		Stores

Note 1: Guaranteed monotonic.

Note 2: Gain error is: [100 x ($V_{F0(MEAS)}$ - ZCE - $V_{F0(IDEAL)}$)/V_{REFH}]; where $V_{F0(MEAS)}$ is the DAC output voltage with input code F0hex. $V_{F0(IDEAL)}$ is the ideal DAC output voltage with input code F0hex (i.e., (V_{REFH} - V_{REFL}) × 240/256 + V_{REFL}).

Note 3: In the voltage range, 0.5V < $V_{OUT\_}$ < V_{DD} - 0.5V.

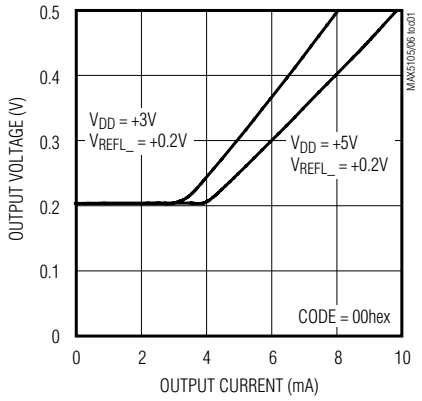
Note 4: Output settling time is measured from the 50% point of the rising edge of last CLK to 1/2LSB of V_{OUT}'s final value for a code transition from 10hex to F0hex. See Figure 4.

Note 5: Channel-to-channel crosstalk is defined as the coupling from one driven reference with input code = FFhex to any other DAC output with the reference of that DAC at a constant value and input code = 00hex.

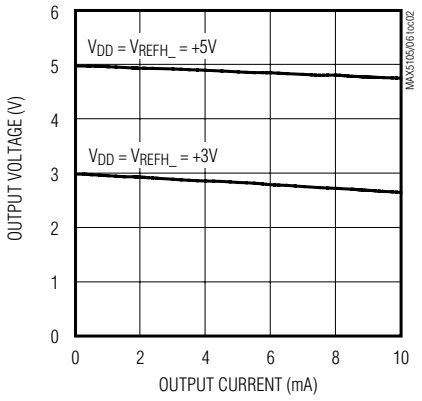
Typical Operating Characteristics

(R_L = ∞, code = FFhex, $V_{REFL\_}$ = GND, T_A = +25°C, unless otherwise noted.)

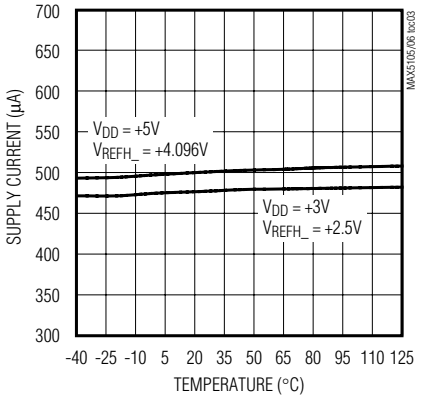
DAC ZERO-CODE OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



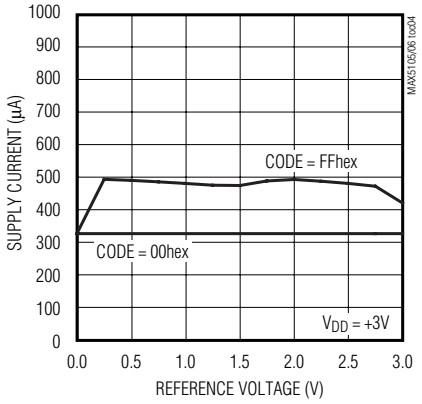
DAC FULL-SCALE OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT



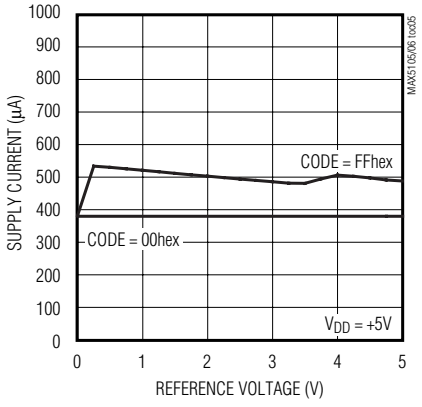
SUPPLY CURRENT vs. TEMPERATURE



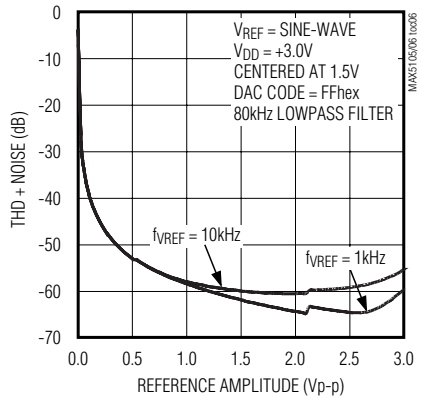
SUPPLY CURRENT vs. REFERENCE VOLTAGE



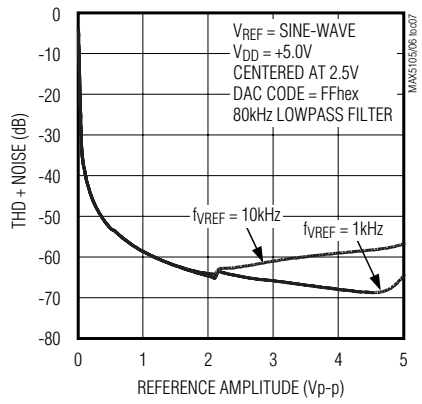
SUPPLY CURRENT vs. REFERENCE VOLTAGE



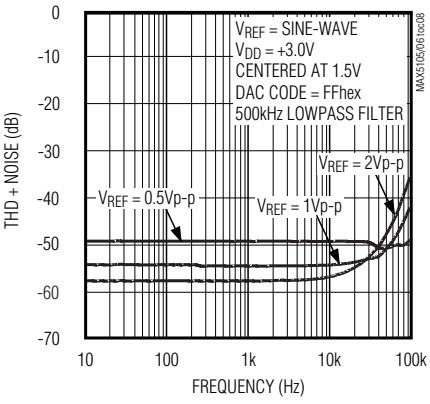
THD + NOISE AT DAC OUTPUT vs. REFERENCE AMPLITUDE



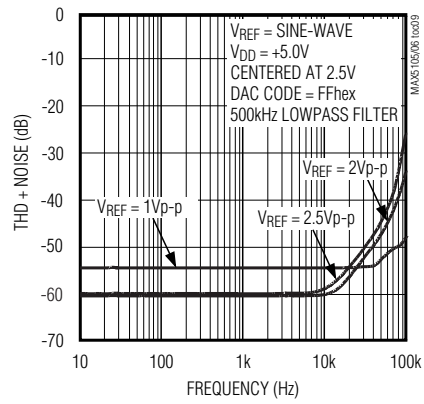
THD + NOISE AT DAC OUTPUT vs. REFERENCE AMPLITUDE



THD + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY



THD + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY

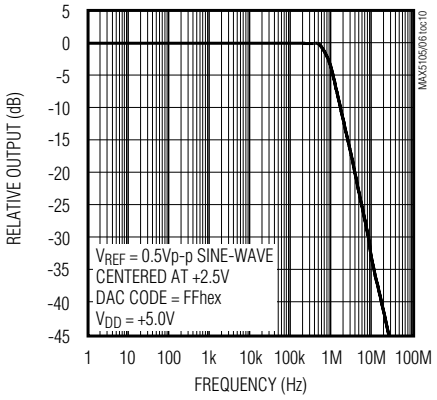


Nonvolatile, Quad, 8-Bit DACs

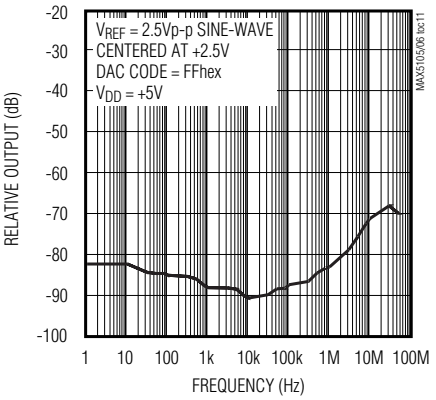
Typical Operating Characteristics (continued)

(R_L = ∞, code = FFhex, $V_{REFL\_}$ = GND, T_A = +25°C, unless otherwise noted.)

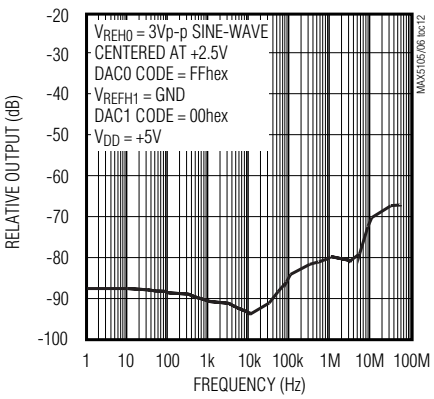
REFERENCE INPUT FREQUENCY RESPONSE



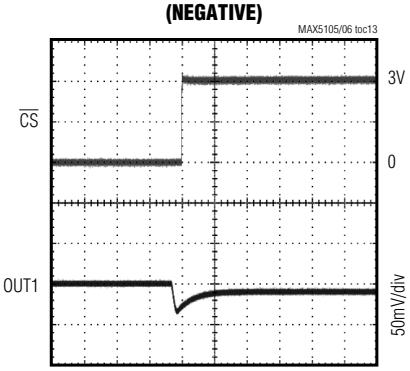
REFERENCE FEEDTHROUGH vs. FREQUENCY



CROSSTALK vs. FREQUENCY

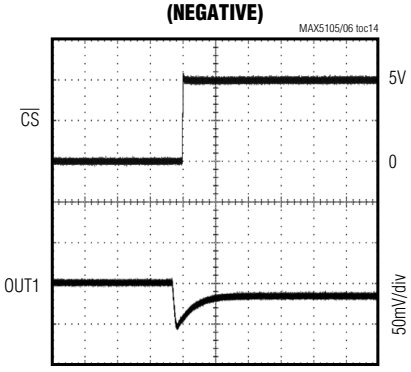


1LSB DIGITAL STEP-CHANGE (NEGATIVE)



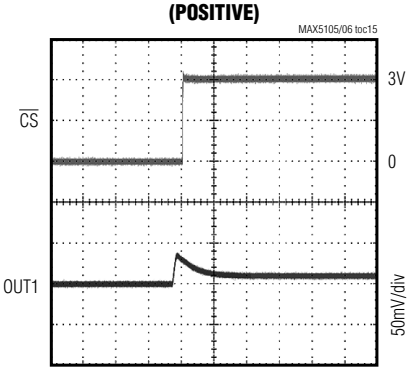
V_{DD} = +3.0V
V_{REFH1} = +2.5V
C_{LOAD} = 100pF
f_{CLK} = 500kHz
CODE = 80 HEX TO 7F HEX
R_L = 10kΩ

1LSB DIGITAL STEP-CHANGE (NEGATIVE)



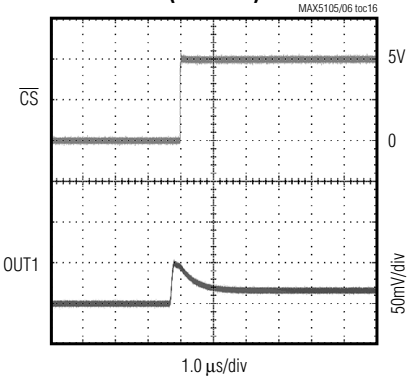
V_{DD} = +5.0V
V_{REFH1} = +4.096V
C_{LOAD} = 100pF
f_{CLK} = 500kHz
CODE = 80 HEX TO 7F HEX
R_L = 10kΩ

1LSB DIGITAL STEP-CHANGE (POSITIVE)



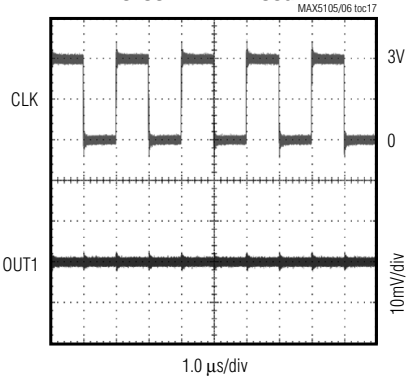
V_{DD} = +3.0V
V_{REFH1} = +2.5V
C_{LOAD} = 100pF
f_{CLK} = 500kHz
CODE = 7F HEX TO 80 HEX
R_L = 10kΩ

1LSB DIGITAL STEP-CHANGE (POSITIVE)



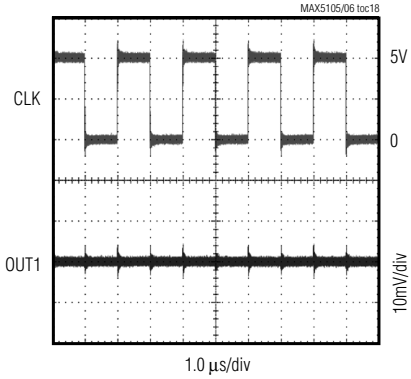
V_{DD} = +5.0V
V_{REFH1} = +4.096V
C_{LOAD} = 100pF
f_{CLK} = 500kHz
CODE = 7F HEX TO 80 HEX
R_L = 10kΩ

CLOCK FEEDTHROUGH



V_{DD} = +3.0V
V_{REFH1} = +2.5V
C_{LOAD} = 100pF
f_{CLK} = 500kHz
CODE = 00 HEX
R_L = 10kΩ

CLOCK FEEDTHROUGH

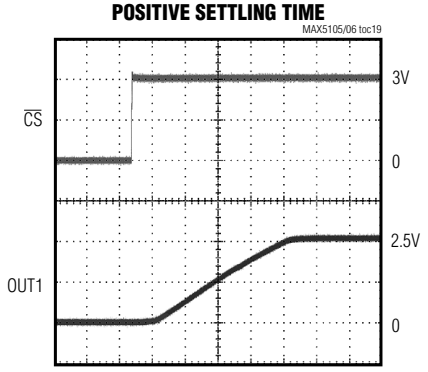


V_{DD} = +5.0V
V_{REFH1} = +4.096V
C_{LOAD} = 100pF
f_{CLK} = 500kHz
CODE = 00 HEX
R_L = 10kΩ

Typical Operating Characteristics (continued)

(R_L = ∞, code = FFhex, $V_{REFL\_}$ = GND, T_A = +25°C, unless otherwise noted.)

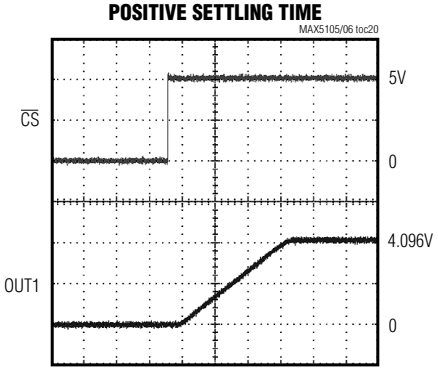
POSITIVE SETTLING TIME



1.0 µs/div

V_{DD} = +3.0V
V_{REFH1} = +2.5V
C_{LOAD} = 100pF
f_{CLK} = 500kHz
CODE = 00 HEX TO FF HEX
R_L = 10kΩ

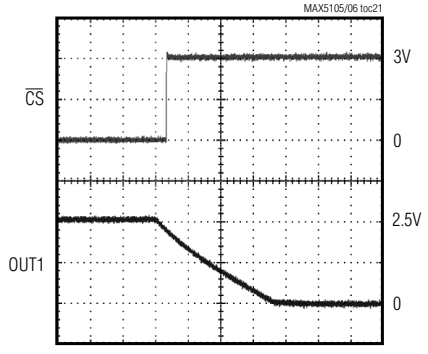
POSITIVE SETTLING TIME



2.0 µs/div

V_{DD} = +5.0V
V_{REFH1} = +4.096V
C_{LOAD} = 100pF
f_{CLK} = 500kHz
CODE = 00 HEX TO FF HEX
R_L = 10kΩ

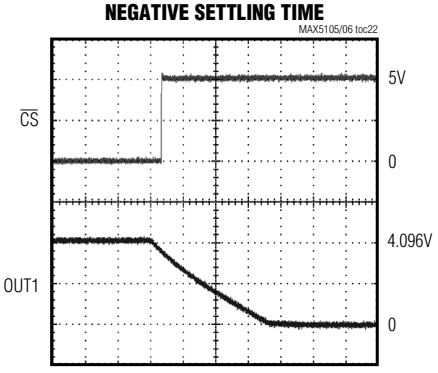
NEGATIVE SETTLING TIME



1.0 µs/div

V_{DD} = +3.0V
V_{REFH1} = +2.5V
C_{LOAD} = 100pF
f_{CLK} = 500kHz
CODE = FF HEX TO 00 HEX
R_L = 10kΩ

NEGATIVE SETTLING TIME



2.0 µs/div

V_{DD} = +5.0V
V_{REFH1} = +4.096V
C_{LOAD} = 100pF
f_{CLK} = 500kHz
CODE = FF HEX TO 00 HEX
R_L = 10kΩ

Pin Description

PIN		NAME	FUNCTION
MAX5105	MAX5106		
1	1	REFH1	DAC1 High Reference Input
2	2	REFH0	DAC0 High Reference Input
3	3	V_{DD}	Positive Supply Voltage
4	—	RDY/$\overline{BSY}$	Ready/Busy Open-Drain Output. Indicates the state of the nonvolatile memory. Connect a 100kΩ pullup resistor from RDY/$\overline{BSY}$ to V_{DD}.
5	4	CLK	Serial Clock Input
6	5	$\overline{CS}$	Chip Select Input
7	6	DIN	Serial Data Input
8	7	DOUT	Serial Data Output
9	—	MUTE	Mute Input. Drives all DAC outputs to their respective REFL_ voltages.
10	8	GND	Ground. Serves as REFL2 and REFL3 for the MAX5106.
11	9	REFL0	DAC0 Low Reference Input
12	10	REFL1	DAC1 Low Reference Input
13	—	REFL2	DAC2 Low Reference Input
14	—	REFL3	DAC3 Low Reference Input
15	11	OUT3	DAC3 Output
16	12	OUT2	DAC2 Output
17	13	OUT1	DAC1 Output
18	14	OUT0	DAC0 Output
19	15	REFH3	DAC3 High Reference Input
20	16	REFH2	DAC2 High Reference Input

Detailed Description

The MAX5105/MAX5106 quad, 8-bit DACs feature an internal, nonvolatile EEPROM, which stores the DAC states for initialization during power-up. These devices consist of four resistor string DACs, four rail-to-rail buffers, a 14-bit shift register, oscillator, power-on reset (POR) circuitry, and five volatile and five nonvolatile memory registers (*Functional Diagram*). The shift register decodes the control and address bits, routing the data to the proper memory registers. Data can be written to a selected volatile register, immediately updating the DAC output, or can be written to a selected nonvolatile register for storage.

The five volatile registers retain data as long as the device is enabled and powered. Once power is removed or the device is shut down, the volatile registers are cleared. The nonvolatile registers retain data even after power is removed. On power-up, the POR circuitry and internal oscillator control the transfer of data from the nonvolatile registers to the volatile registers, which automatically initializes the device upon startup. Data can be read from the nonvolatile registers through DOUT.

Table 1. Mute/Shutdown Register Mapping

Bit in Register	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
Controlling Function	Mute DAC3	Mute DAC2	Mute DAC1	Mute DAC0	Shutdown DAC3	Shutdown DAC2	Shutdown DAC1	Shutdown DAC0

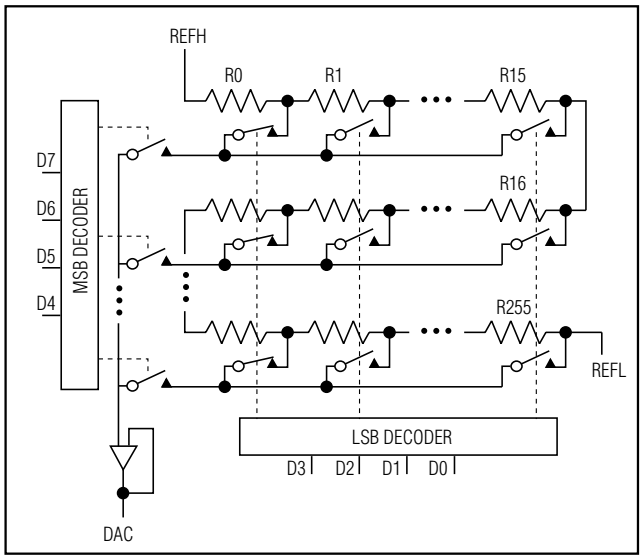


Figure 1. DAC Simplified Circuit Diagram

DAC Operation

The MAX5105/MAX5106 use a matrix decoding architecture for the DACs, which saves power in the overall system. A resistor string placed in a matrix fashion divides down the difference between the external reference voltages, V_{REFH} and V_{REFL}. Row and column decoders select the appropriate tab from the resistor string, providing the needed analog voltages. The resistor string presents a code-independent input impedance to the reference and guarantees a monotonic output. Figure 1 shows a simplified diagram of one of the four DACs.

Output Buffer Amplifiers

All MAX5105/MAX5106 analog outputs are internally buffered by precision unity-gain followers that slew at about 0.5V/µs. The outputs can swing from GND to V_{DD}. With a $V_{REFL\_}$ to $V_{REFH\_}$ (or $V_{REFH\_}$ to $V_{REFL\_}$) output transition, the amplifier outputs typically settle to ±1/2LSB in 6µs when loaded with 10kΩ in parallel with 100pF.

The software mute/shutdown command independently drives each output to its respective REFL_ voltage (mute) or to a high-impedance state (shutdown). Placing all four DACs in shutdown reduces supply current to 10µA (max). The MAX5105 also provides an asynchronous MUTE input, simultaneously driving all DAC outputs to their respective REFL_ voltages.

Internal EEPROM

The MAX5105/MAX5106 internal EEPROM consists of five nonvolatile registers that retain the DAC output and operating states after the device is powered down. Four registers store data for each DAC, and one stores the mute and shutdown states for the device.

DAC Registers

The MAX5105/MAX5106 have eight 8-bit DAC registers, four volatile and four nonvolatile, that store DAC data. The four volatile DAC registers hold the current value of each DAC. Data is written to these registers in two ways: directly from DIN or loaded from the respective nonvolatile registers (see *Serial Input Data Format and Control Codes*). These registers are cleared when the device is shut down or power is removed.

The four nonvolatile registers retain the DAC values even after power is removed. Stored data is accessed in two ways: transferring data to a volatile register to update the respective DAC output or reading data through DOUT (see *Serial Input Data Format and Control Codes*). On power-up, the device is automatically initialized with data stored in the nonvolatile registers.

Mute/Shutdown Registers

The MAX5105/MAX5106 have two 8-bit mute/shutdown registers that store the operating state of each DAC. The four MSBs hold the mute states, and the four LSBs hold the shutdown states (Table 1). The volatile registers hold the current mute/shutdown state of each DAC. Like the DAC registers, the nonvolatile mute/shutdown register maintains its data after the device is powered down, and the contents can be read on DOUT. The volatile register is initialized with the nonvolatile data on power-up and can be loaded through DIN or from the nonvolatile register (see *Serial Input Data Format and Control Codes*).

Table 2. Serial Interface Programming Commands

14-BIT SERIAL WORD							FUNCTION
START	C1	C0	A2	A1	A0	D7–D0	
1	0	0	0	0	0	8-bit DAC data	Write DAC data to DAC0 nonvolatile register. Output remains unchanged.
1	0	0	0	0	1	8-bit DAC data	Write DAC data to DAC1 nonvolatile register. Output remains unchanged.
1	0	0	0	1	0	8-bit DAC data	Write DAC data to DAC2 nonvolatile register. Output remains unchanged.
1	0	0	0	1	1	8-bit DAC data	Write DAC data to DAC3 nonvolatile register. Output remains unchanged.
1	0	0	1	0	0	8-bit DAC data	Write shutdown and mute states to nonvolatile register. A 1 in bits D7–D4 mutes the respective DAC; a 1 in bits D3–D0 shuts down the respective DAC (Table 1). Outputs remain unchanged.
1	0	1	0	0	0	8-bit DAC data	Write DAC data to DAC0 volatile register and update OUT0. All other DAC outputs remain unchanged.
1	0	1	0	0	1	8-bit DAC data	Write DAC data to DAC1 volatile register and update OUT1. All other DAC outputs remain unchanged.
1	0	1	0	1	0	8-bit DAC data	Write DAC data to DAC2 volatile register and update OUT2. All other DAC outputs remain unchanged.
1	0	1	0	1	1	8-bit DAC data	Write DAC data to DAC3 volatile register and update OUT3. All other DAC outputs remain unchanged.
1	0	1	1	0	0	8-bit DAC data	Write shutdown and mute states to volatile register. A 1 in bits D7–D4 mutes the respective DAC; a 1 in bits D3–D0 shuts down the respective DAC (Table 1). DAC outputs updated to their respective mute/shutdown states.
1	1	0	0	0	0	XXXXXXXX	Read DAC0 nonvolatile register. Contents of DAC0 nonvolatile register available on DOUT. D7–D0 are ignored, and all DAC outputs remain unchanged.
1	1	0	0	0	1	XXXXXXXX	Read DAC1 nonvolatile register. Contents of DAC1 nonvolatile register available on DOUT. D7–D0 are ignored, and all DAC outputs remain unchanged.
1	1	0	0	1	0	XXXXXXXX	Read DAC2 nonvolatile register. Contents of DAC2 nonvolatile register available on DOUT. D7–D0 are ignored, and all DAC outputs remain unchanged.
1	1	0	0	1	1	XXXXXXXX	Read DAC3 nonvolatile register. Contents of DAC3 nonvolatile register available on DOUT. D7–D0 are ignored, and all DAC outputs remain unchanged.
1	1	0	1	0	0	XXXXXXXX	Read mute/shutdown nonvolatile register. Contents of mute/shutdown nonvolatile register available on DOUT. D7–D0 are ignored, and all DAC outputs remain unchanged.

Table 2. Serial Interface Programming Commands (continued)

14-BIT SERIAL WORD							FUNCTION
START	C1	C0	A2	A1	A0	D7–D0	
1	1	1	0	0	0	XXXXXXXX	Load DAC0 nonvolatile register. Contents of DAC0 nonvolatile register are loaded into the corresponding volatile register and OUT0 updated. D7–D0 are ignored, and all other DAC outputs remain unchanged.
1	1	1	0	0	1	XXXXXXXX	Load DAC1 nonvolatile register. Contents of DAC1 nonvolatile register are loaded into the corresponding volatile register and OUT1 updated. D7–D0 are ignored, and all other DAC outputs remain unchanged.
1	1	1	0	1	0	XXXXXXXX	Load DAC2 nonvolatile register. Contents of DAC2 nonvolatile register are loaded into the corresponding volatile register and OUT2 updated. D7–D0 are ignored, and all other DAC outputs remain unchanged.
1	1	1	0	1	1	XXXXXXXX	Load DAC3 nonvolatile register. Contents of DAC3 nonvolatile register are loaded into the corresponding volatile register and OUT3 updated. D7–D0 are ignored, and all other DAC outputs remain unchanged.
1	1	1	1	0	0	XXXXXXXX	Load mute/shutdown nonvolatile register. Contents of mute/shutdown nonvolatile register are loaded into the mute/shutdown volatile register, and all DACs are placed into their respective mute/shutdown states. D7–D0 are ignored.

Serial Interface

The MAX5105/MAX5106 communicate with microprocessors (µPs) through a synchronous, full-duplex 3-wire interface (Figure 2). Data is sent MSB first and is transmitted in one 14-bit word. A 4-wire interface adds a line for RDY/$\overline{BSY}$ (MAX5105), indicating the status of the nonvolatile memory. Data is transmitted and received simultaneously.

Figure 3 shows the detailed serial interface timing. Note that the clock should be low if it is stopped between updates. DOUT is high impedance until a valid read command and address is written to the device.

Serial data is clocked into the 14-bit shift register in an MSB-first format, with the start-bit, configuration, and address information preceding the actual DAC data. Data is clocked in on CLK's rising edge while $\overline{CS}$ is low.

$\overline{CS}$ must be low to enable the device. If $\overline{CS}$ is high, the interface is disabled and DOUT remains unchanged. $\overline{CS}$ must go low at least 100ns before the first rising edge of the clock pulse to properly clock in the first bit. With $\overline{CS}$ low, data is clocked into the shift register on the rising edge of the external serial clock.

Serial Input Data Format and Control Codes

The 14-bit serial input format, shown in Figure 4, comprises one start bit, two control bits (C0, C1), three address bits (A0, A1, A2), and eight data bits (D7–D0). The 5-bit address/control code configures the DAC as shown in Table 2.

Nonvolatile Store Command

The nonvolatile store command loads the 8-bit DAC data into the selected nonvolatile DAC register, or the DAC operating states into the mute/shutdown nonvolatile register. The nonvolatile store command does not affect the current DAC outputs or operating states. Once the control and address bits are clocked in, RDY/$\overline{BSY}$ (MAX5105) goes low until the nonvolatile store operation is complete. For the MAX5106, wait the maximum 13ms store time before writing a new word to the device. Do not write new data to the device until RDY/$\overline{BSY}$ (MAX5105) returns high, or the 13ms store time (MAX5106) has elapsed. Figure 5 shows the nonvolatile store command timing diagram.

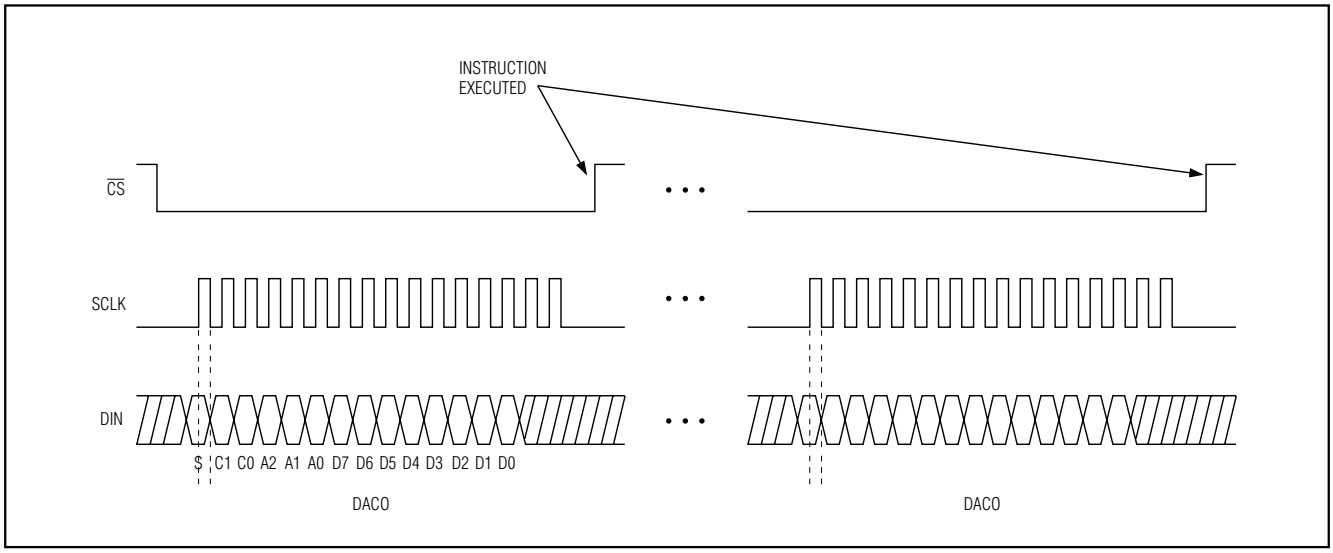


Figure 2. 3-Wire Interface Timing

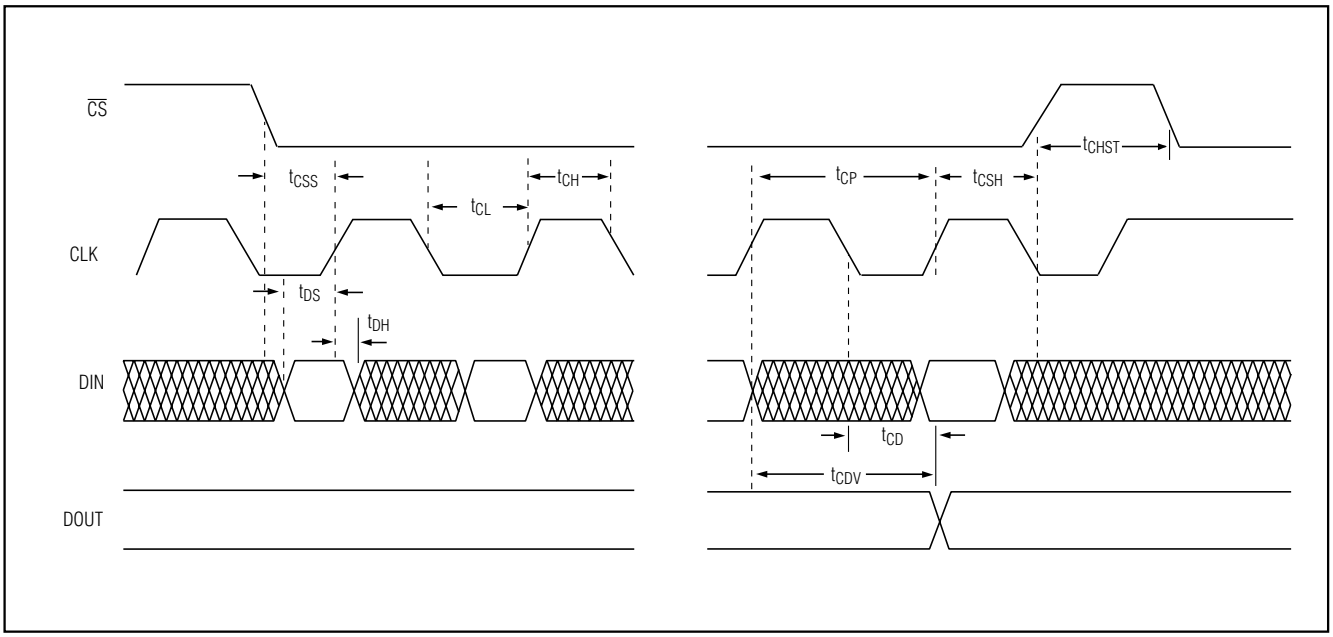


Figure 3. Detailed Serial-Interface Timing Diagram

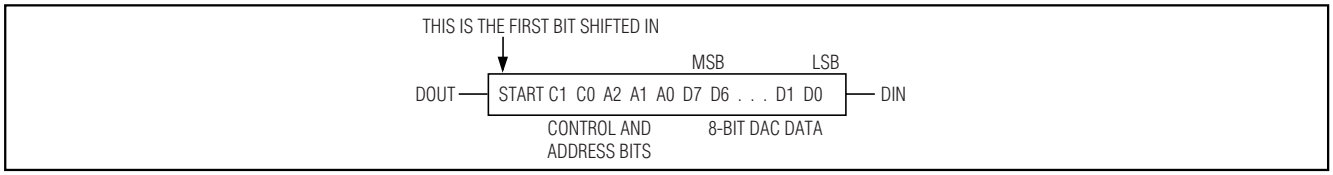


Figure 4. Serial Input Format

Table 3. Nonvolatile Store Command

START	C1	C0	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	Address			8-Bit Data							

Table 4. Register Write Command

START	C1	C0	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Address			8-Bit Data							

Table 5. Nonvolatile Read Command

START	C1	C0	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Address			Don't Care							

Table 6. Nonvolatile Load Command

START	C1	C0	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	Address			Don't Care							

Table 7. Mute/Shutdown Modes

START	C1	C0	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	Mute/Shutdown State							

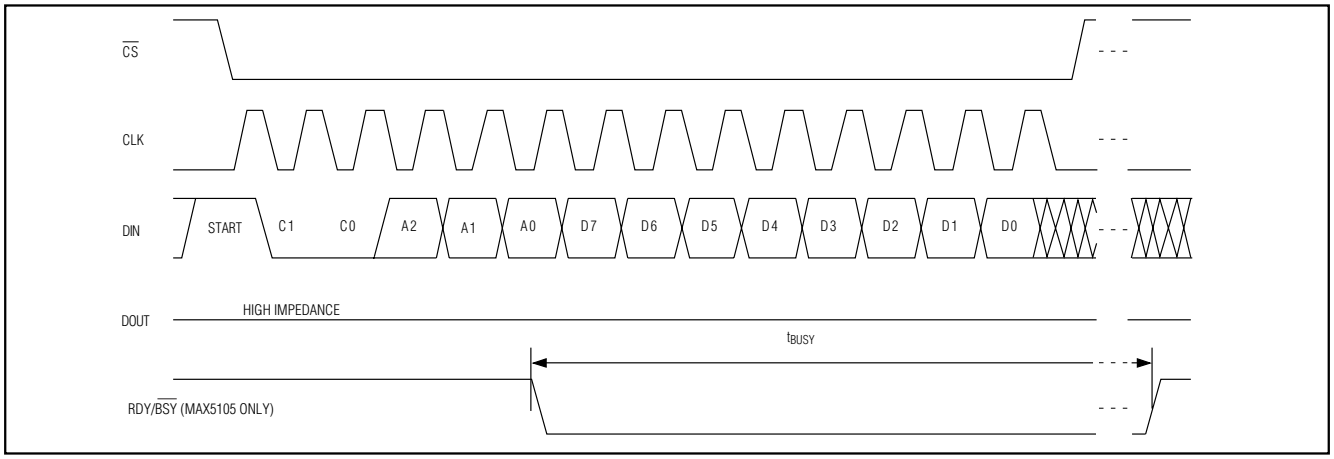


Figure 5. Nonvolatile Store Command Timing Diagram

The nonvolatile store command is ignored if all DACs are muted or in shutdown.

Register Write Command

This command directly loads the DAC data to the selected DAC volatile register and updates the respective output on the rising edge CLK corresponding to D0. The mute/shutdown volatile register is also accessible through this command by setting A2 high. A 1 in any of the four MSBs (D7–D4) mutes the selected DAC; a 1 in any of the four LSBs (D3–D0) disables the selected DAC (Table 1). The DAC operating states change

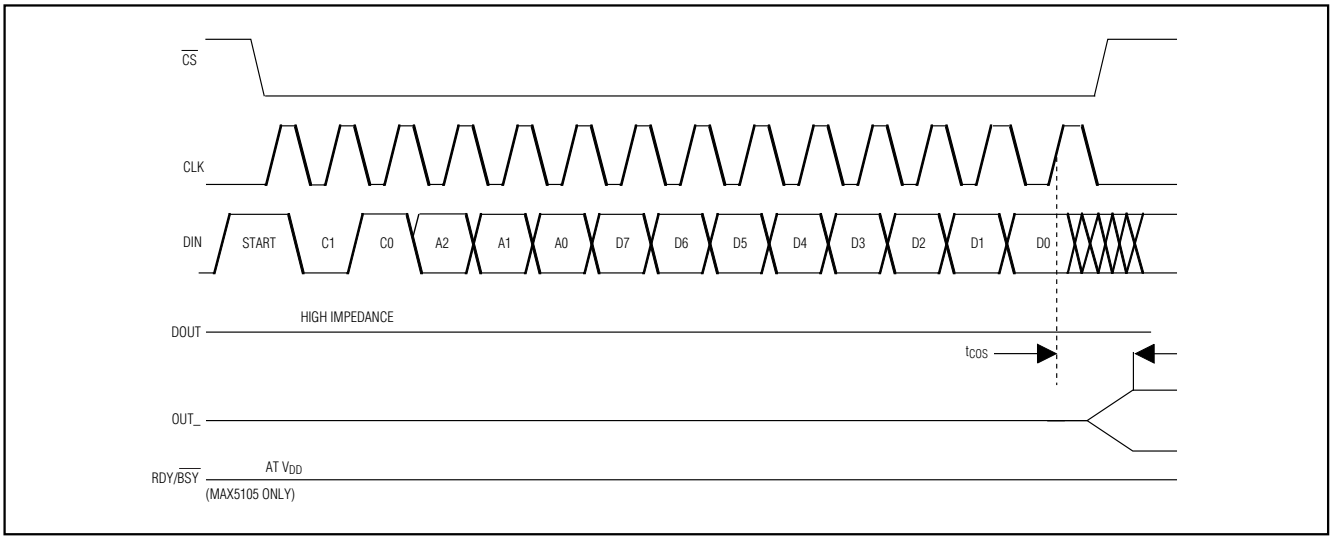


Figure 6. Register Write Command Timing Diagram

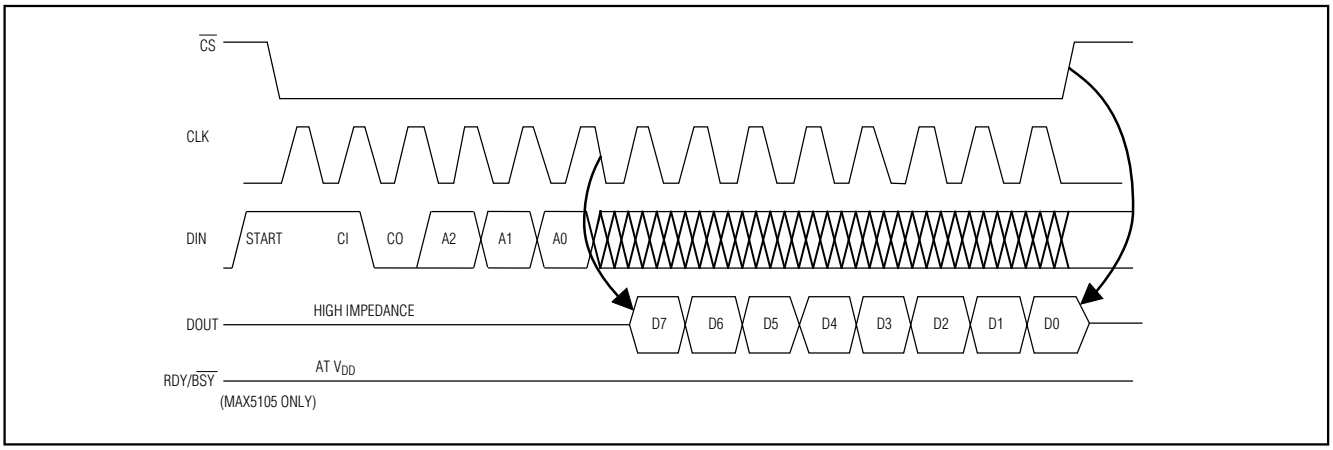


Figure 7. Nonvolatile Read Command Timing Diagram

on the rising edge of CLK corresponding to D0. The register write command does not affect data stored in the nonvolatile memory. Figure 6 shows the register write command timing diagram.

Nonvolatile Read Command

The nonvolatile read command makes the data from the selected nonvolatile register available to external devices. Data is clocked out on DOUT during the eight clock cycles following A0. DOUT returns to a high-impedance state when $\overline{CS}$ goes high. This command has no effect on the DAC outputs, operating states, or contents of the nonvolatile registers. Figure 7 shows the nonvolatile read command timing diagram. RDY/$\overline{BSY}$ remains high while a read is taking place.

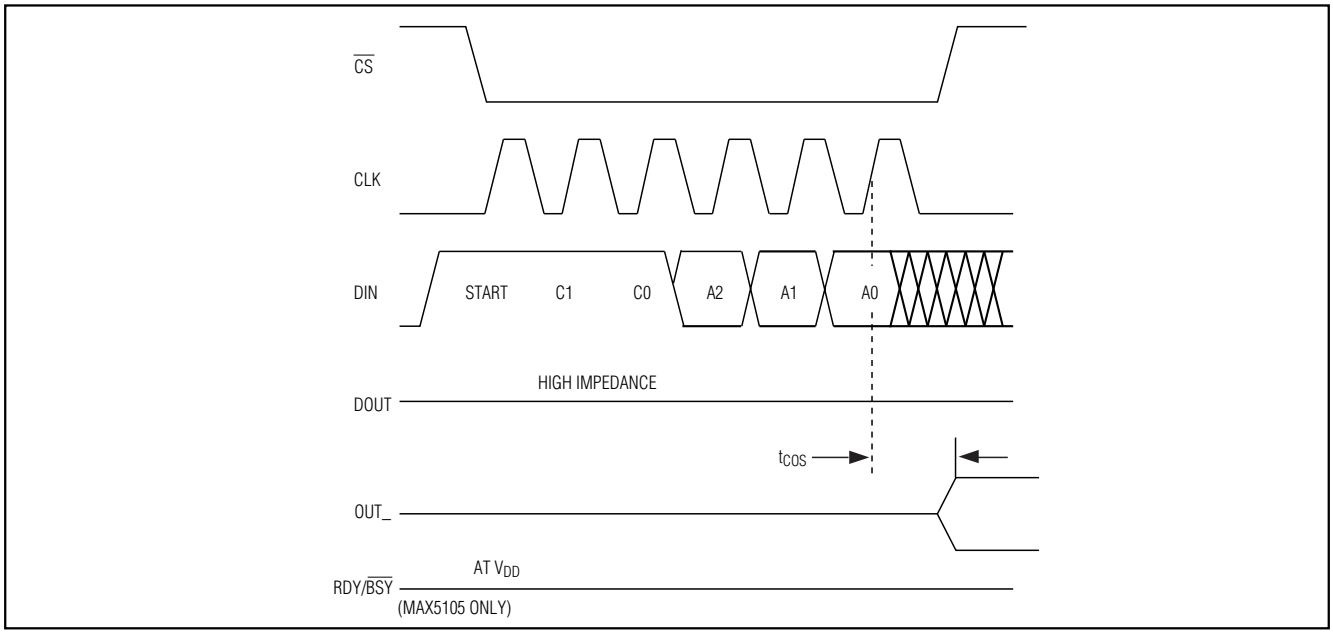


Figure 8. Nonvolatile Load Command Timing Diagram

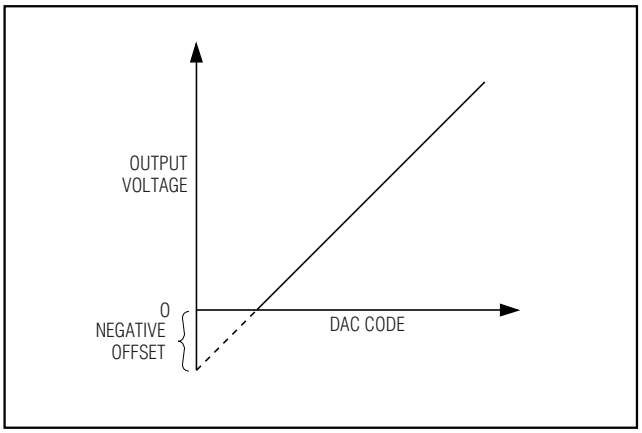


Figure 9. Effect of Negative Offset (Single Supply)

Nonvolatile Load Command

The nonvolatile load command writes the contents of the selected nonvolatile register to the corresponding volatile register during the eight clock cycles following A0. This updates the respective DAC output or changes the operating state of the device on the rising edge of CLK corresponding to A0. This command does not affect the data in the nonvolatile register. Figure 8 shows the nonvolatile load command timing diagram. RDY/$\overline{BSY}$ remains high while a volatile register load is taking place.

Mute/Shutdown Modes

The MAX5105/MAX5106 feature software-controlled mute and shutdown modes. The shutdown mode places the DAC outputs in a high-impedance state and reduces quiescent current consumption to 10µA (max) with all DACs disabled.

Mute drives the selected DAC output to the corresponding REFL_ voltage. The volatile DAC register retains its data, and the output returns to its previous state when mute is removed. The MAX5105 also features an asynchronous MUTE input that mutes all DACs.

The output buffers are individually disabled/muted with ones in the proper data bits (D7–D0) (Table 1).

When all DACs are muted or shut down, the nonvolatile store command is ignored. If the mute/shutdown novolatile register is used to shut down or mute all of the DACs, use the register write command to change the operating state of the device. Do this by executing a register write command that changes the contents of the mute/shutdown volatile register. Following this, the nonvolatile store command is again recognized.

Power-On Reset

The power-on reset (POR) controls the initialization of the MAX5105/MAX5106. During this time, the on-chip oscillator is enabled and used to load the volatile DAC and mute/shutdown registers with data from the EEPROM.

This initialization period takes about 80µs with the DAC registers loading first and the mute/shutdown register loading last. During this time, the DAC outputs are held in the mute state and the serial interface is disabled. Once the mute/shutdown register is loaded, the DAC outputs are updated to their stored data and operating states, and the serial interface is enabled.

Applications Information

DAC Linearity and Offset Voltage

The output buffer can have a negative input offset voltage that would normally drive the output negative, but since there is no negative supply, the output remains at GND (Figure 9). When linearity is determined using the end-point method, it is measured between code 10 (0Ahex) and full-scale code (FFhex) after the offset and gain error are calibrated out. With a single supply, negative offset causes the output not to change with an input code transition near zero (Figure 9). Thus, the lowest code that produces a positive output is the lower endpoint.

External Voltage Reference

The MAX5105/MAX5106 have two reference inputs for each DAC, REFH_, and REFL_. REFH_ sets the full-scale voltage, while REFL_ sets the zero code output. REFL2 and REFL3 are internally connected to GND in the MAX5106. A 256kΩ typical input impedance at REFH_ is code independent. The output voltage from these devices can be represented by a digitally programmable voltage source as follows:

$$V_{OUT} = [(V_{REFH\_} - V_{REFL\_}) \times (N / 256)] + V_{REFL\_}$$

where N is the decimal value of the DAC's binary input code.

Power Sequencing

The voltage applied to REFH_ and REFL_ should not exceed V_{DD} at any time. If proper power sequencing is not possible, connect an external Schottky diode between REFH_ and REFL_ and V_{DD} to ensure compliance with the absolute maximum ratings. Do not apply signals to the digital inputs before the device is fully powered up.

Power-Supply Bypassing and Ground Management

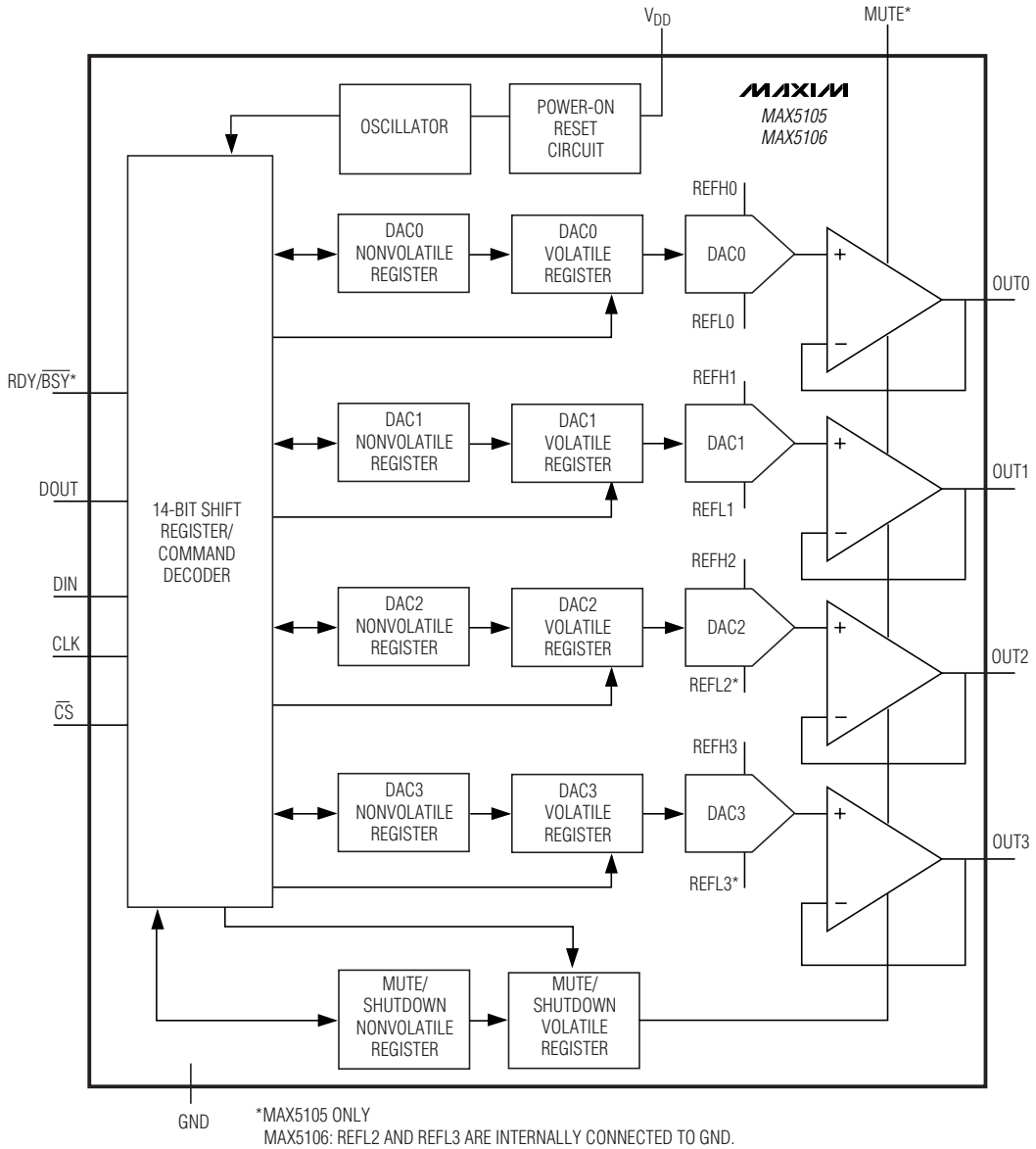
Digital or AC transient signals on GND can create noise at the analog output. Return GND to the highest-quality ground available. Bypass V_{DD} with a 0.1µF capacitor, located as close to the device as possible. Bypass REF_ to GND with a 0.1µF capacitor. Carefully printed circuit board ground layout minimizes crosstalk between the DAC outputs and digital inputs.

Chip Information

TRANSISTOR COUNT: 32,000

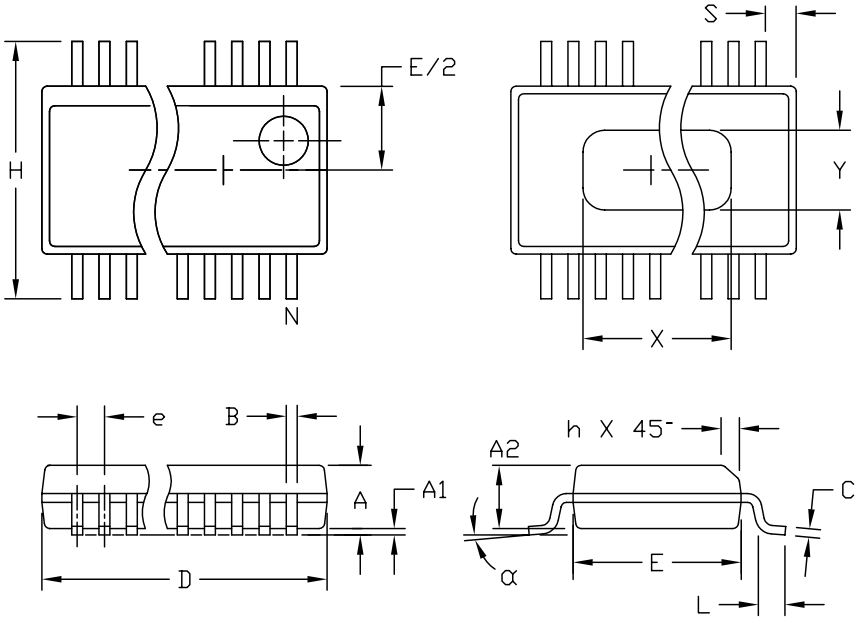
PROCESS: CMOS

Functional Diagram



Nonvolatile, Quad, 8-Bit DACs

Package Information



QSOP.EPS

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006″ PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.
5. MEETS JEDEC MO137.

MAXIM

PROPRIETARY INFORMATION

TITLE:

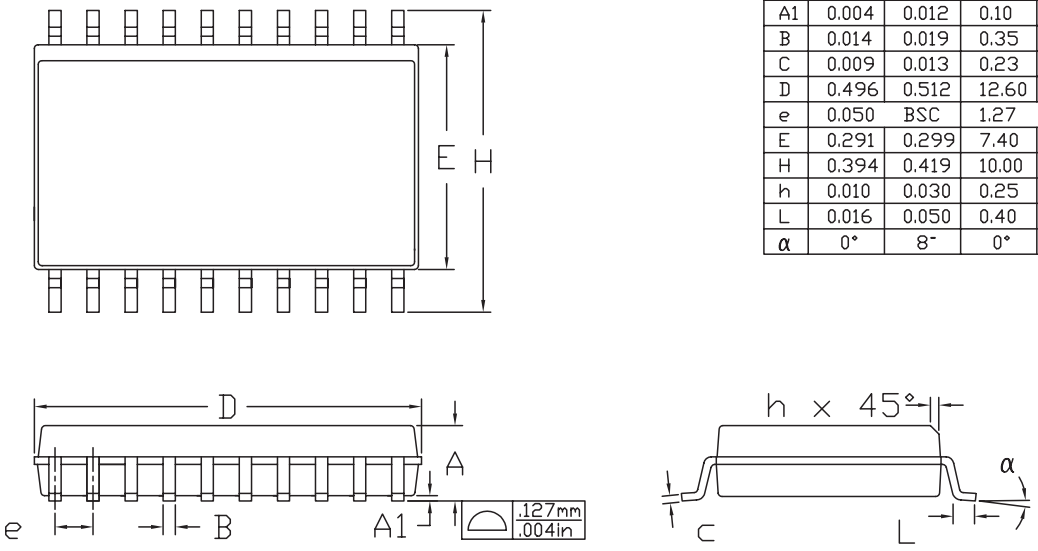
PACKAGE OUTLINE, QSOP, .150″, .025″ LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	C	1/1

Package Information (continued)

20L, SOIC.EPS

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
D	0.496	0.512	12.60	13.00
e	0.050	BSC	1.27	BSC
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°



NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-013 AC

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 20L SOIC

APPROVAL	DWG	REV	
	21-0334	B	1/1